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(54) Multiplying digital-to-analogue converter.

(57) A multiplying digital-to-analogue converter is of the kind in which digitally weighted currents proportional to a voltage applied to an analogue input (19) are generated at respective outputs (3) of a current mirror arrangement (1), these currents being switched to an output (9) in accordance with the value of a digital signal applied to a digital input (11). In order that the converter can accommodate analogue input voltage of either polarity relative to ground and generate corresponding output currents a bias current is applied to the current mirror input (2) from a current source (15). This results in digitally weighted bias currents being generated at the current mirror outputs (3). These bias currents are offset by corresponding bias currents generated at respective outputs (6) of a second current mirror arrangement (4).

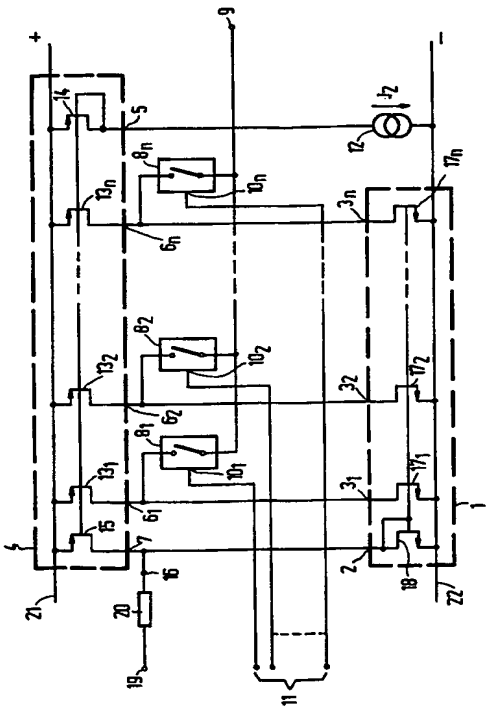

FIG.1

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EUROPEAN SEARCH REPORT

Application Number
EP 92 20 3330

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	US-A-4 168 528 (COMER) * column 4, line 3 - column 5, line 40; figure 3 *	1	H03M1/74 G06J1/00
A	PROCEEDINGS OF THE 1989 BIPOLAR CIRCUITS AND TECHNOLOGY MEETING 18 September 1989 , MINNEAPOLIS MARRIOTT CITY CENTER HOTEL pages 52 - 55 XP000089827 MARTINEZ ET AL 'a monolithic 12-bit multiplying dac for ntsc and hdtv applications' * page 52, column 2 - page 53, column 1; figures 1,2 *	1	
P,A	US-A-5 128 674 (KONG ET AL) * abstract *	1	
A	US-A-4 384 274 (MAO) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H03M
G06J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	3 March 1994	Guivol, Y

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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E : earlier patent document, but published on, or after the filing date
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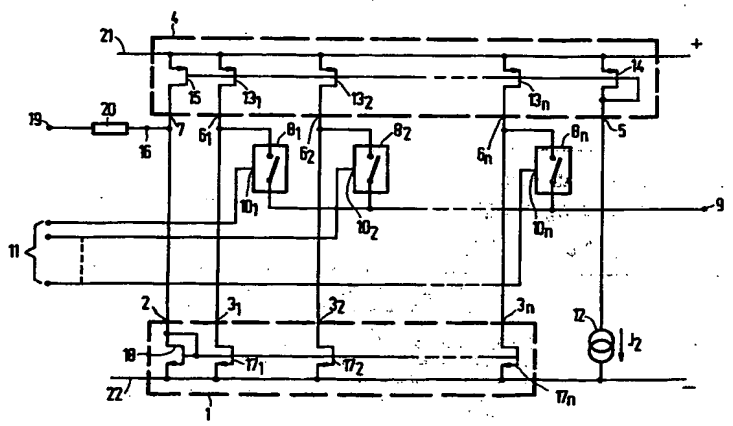

FIG.1

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This invention relates to a multiplying digital-to-analogue converter circuit arrangement comprising a current mirror arrangement constructed to generate currents $-2^{-1}I_1, -2^{-2}I_1, ..., -2^{-n}I_1$ at first, second,....nth outputs respectively thereof in response to the application of a current J_1 to an input thereof, where I_1 is in a predetermined ratio to J_1, and a respective controllable switch coupling each said output to an output of the converter circuit arrangement, control inputs of said switches collectively constituting the digital signal input of said converter circuit arrangement.

Known such converter circuit arrangements are disclosed in, for example, IBM Technical Disclosure Bulletin Vol. 24, No. 5, (October 1981) at pages 2342-2344, and in JP-A-61-2427. Each of these known converter arrangements generates a current at its output when a current is applied to the current mirror input and at least one of the switches is closed, the output current being proportional to both the mirror input current and the number represented by the digital code constituted by the configuration of closed and open switches prevailing at the relevant time. The input currents to the current mirror arrangements of these known converters must always have a specific polarity if the mirror arrangements are to operate correctly, and it will be evident moreover that the output currents of these known converters always too have a specific polarity, whatever the value of the mirror input current and/or the configuration of open and closed switches actually is.

In some possible applications for multiplying digital-to-analogue converts there is a requirement that the converter be capable of operating with analogue input signal currents of either polarity and generating output currents having a polarity which is governed by that of the input signal current regardless of what the particular value of the converter digital input signal is at the relevant time. If an analogue signal current input is coupled to an input of the current mirror arrangement of either of the known converter arrangements and, moreover, a forward bias current is applied to an input of the relevant current mirror arrangement, then the current mirror arrangement can be made to operate with analogue input signal currents of either polarity. However, the converter output current will still always have the same polarity, regardless of the polarity of the input signal current. Addition of a fixed opposing bias current to the converter output current will not solve this problem because, although it makes possible the production of resulting output currents of either polarity, these polarities can only be correctly governed by those of the input signal current for one specific value of the converter digital input signal.

In order to provide a solution to this problem in the case of generalized multiplying digital-to-analogue converters JP-A-60-241307 discloses a converter arrangement which includes two mutually identical complete multiplying digital-to-analogue converters. Both converters are fed with the same digital input signal at all times, i.e. their digital signal inputs are connected in parallel. The analogue input of the first converter is fed with both an analogue input signal current and a bias current as postulated above, whereas the analogue input of the second converter is fed only with a bias current which is identical to that fed to the analogue input of the first converter. The analogue output current of the second converter is sign-reversed and the result is added as a bias to the analogue output current of the first converter. Thus the biassing of the output current of the first converter is adjusted in accordance with the value of the digital input signal to the arrangement in such a way that the resulting output current (which constitutes the arrangement output) always has the correct sign relationship to the sign of the analogue input signal current to the arrangement. The effect on the output current of the first converter of the biassing of its input current is always exactly cancelled by the addition thereto of the sign-reversed output current of the second converter, regardless of the value of the digital input signal of the arrangement.

The use of two complete multiplying digital-to-analogue converters in the arrangement of JP-A-60-241307 can be rather costly, and it is an object of the present invention to provide an arrangement which can give equivalent results with less complex circuitry.

The invention provides a multiplying digital-to-analogue converter circuit arrangement of the kind defined in the first paragraph which is characterized in that it includes a second current mirror arrangement constructed to generate currents $2^{-1}I_2, 2^{-2}I_2, ..., 2^{-n}I_2$ at first, second,....nth outputs respectively thereof in response to the application of a current $-J_2$ to an input thereof, where I_2 is in a predetermined ratio to J_2, d.c. connections between the first, second,....nth outputs of said second current mirror arrangement and the first, second,....nth outputs respectively of the first-mentioned current mirror arrangement, a direct current source connected to the input of said first-mentioned current mirror arrangement for applying a bias current J_1 thereto, a direct current source connected to the input of said second current mirror arrangement for applying a bias current thereto which is such as to result in the generation of currents $2^{-1}I_1, 2^{-2}I_1, ...2^{-n}I_1$ at the first, second,....nth outputs respectively of said second current mirror arrangement, and an analogue signal current input connected to the input of said first-

mentioned current mirror arrangement. It should be noted that the presence of minus signs in front of some of the currents referred to and not in front of others, is to be understood to denote merely the relative polarities of the various currents and not their absolute polarities, the latter being dependent at will on whatever sign is chosen to be appropriate to denote, for example, the flow of conventional current into (as compared with out of) a node.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings, in which

Figure 1 is the circuit diagram of a simple first embodiment, and

Figure 2 is the circuit diagram of a second embodiment which includes various refinements compared with that of Figure 1.

In Figure 1, a multiplying digital-to-analogue converter circuit arrangement comprises a first current mirror arrangement 1 having an input 2 and n outputs $3_1,3_2,....3_n$, a second current mirror arrangement 4 having an input 5, n outputs $6_1,6_2,....6_n$ and a further output 7, and n controllable switches $8_1,8_2,....8_n$ which couple the outputs $3_1,3_2,....3_n$ respectively of the mirror 1 to the output 9 of the converter arrangement. The switches $8_1,8_2,....8_n$ (which may be constituted by transistor switches) have control inputs $10_1,10_2,....10_n$ respectively which collectively constitute the digital signal input 11 of the converter arrangement. The outputs $3_1,3_2,....3_n$ of the mirror arrangement 1 are d.c.-connected to the outputs $6_1,6_2,....6_n$ respectively of the mirror arrangement 4, and the further output 7 of the mirror arrangement 4 is d.c.-connected to the input 2 of the mirror arrangement 1. The input 5 of the mirror arrangement 4 is fed with a current $-J_2$ by means of a direct current source 12 connected thereto. This results in currents $2^{-1}I_2,2^{-2}I_2,....2^{-n}I_2$ being generated at the outputs $6_1,6_2,....6_n$ respectively of the mirror arrangement 4, and in a current J_1 being generated at the further output 7, where I_2 is in a predetermined ratio R_1 to J_2, and J_1 is in a predetermined ratio R_2 to J_2. (R_1 and R_2 may or may not be equal to each other). To this end the sizes of the transistors $13_1,13_2,....13_n$ whose drains feed the outputs $6_1,6_2,....6_n$ respectively are chosen in known manner to be in the ratios $2^{-1}R_1,2^{-2}R_1,....,2^{-n}R_1$ respectively to the size of the diode-connected transistor 14 which is fed from the input 5, and the size of the transistor 15 which feeds the output 7 is chosen to be in the ratio R_2 to the size of the transistor 14.

The output 7 of mirror arrangement 4 is used as a direct current source for supplying the input 2 of mirror arrangement 1 with a bias current J_1. Mirror arrangement 1 responds to the bias current J_1 by generating currents $-2^{-1}I_1,-2^{-2}I_1,....,-2^{-n}I_1$ at its outputs $3_1,3_2,....3_n$ respectively, where I_1 is in a predetermined ratio R_3 to J_1. (R_3 may or may not be equal to R_1 and/or R_2). To this end the sizes of the transistors $17_1,17_2,....17_n$ whose drains feed the outputs $3_1,3_2,....3_n$ respectively are chosen in known manner to be in the ratios $2^{-1}R_3,2^{-2}R_3,....2^{-n}R_3$ to the size of the diode-connected transistor 18 which is fed from the input 2. It is arranged moreover that under the conditions at present being described, i.e. with no current i passing to or from the input 2 of mirror arrangement 1 via a signal current input terminal 16, the currents generated at the outputs $6_1,6_2,....6_n$ of mirror circuit 4 are exactly matched by those sunk at the outputs $3_1,3_2,....3_n$ respectively of mirror circuit 1, so that no current will be transferred to the output 9 of the converter arrangement in the event of any of the switches 8 being closed. Thus it is arranged that $I_2 = I_1$, which implies that $R_2.R_3 = R_1$. The relative sizes of the transistors 13,15,17 and 18 are therefore chosen so that this last condition is satisfied.

If now a positive signal current i is applied to the signal current input 16 from a signal voltage input 19 via a high-value resistor 20 the current fed to the input 2 of mirror arrangement 1 will increase, resulting in mirror 2 attempting to increase the currents sunk at each of its outputs 3. Now if any of the switches 8 are closed this will result in current being drawn to the relevant output(s) 3 from the output terminal 9. If on the other hand the signal current is negative the opposite effect will occur; the excess of the currents generated at the relevant outputs 6 of mirror 4 over that now being sunk by the relevant outputs 3 of mirror arrangement 1 will pass to output 9 via any closed switch 8.

The input voltage applied to input 19 should obviously be referred to a voltage level lying midway between the potentials on the positive and negative supply rails 21 and 22 respectively, and the converter output current at terminal 9 should also be sunk/sourced at this voltage level. The latter can be conveniently achieved by connecting the terminal 9 to the so-called "virtual earth" inverting input of an operational amplifier provided with a feedback path from its output to its inverting input, this amplifier having its power supply input connected between the supply rails 21 and 22.

In the embodiment of Figure 2 various components have been given, where appropriate, the same references as their counterparts in Figure 1.

One way in which the embodiment of Figure 2 differs from that of Figure 1 is that the current mirror 1 employs in known manner a group of interconnected transistors 30,31,32 and 33 instead of the simple diode-connected transistor 18 of Figure 1, to obtain improved accuracy. Accuracy is

mentioned current mirror arrangement to the output of the converter circuit arrangement and to a reference potential point as alternatives.

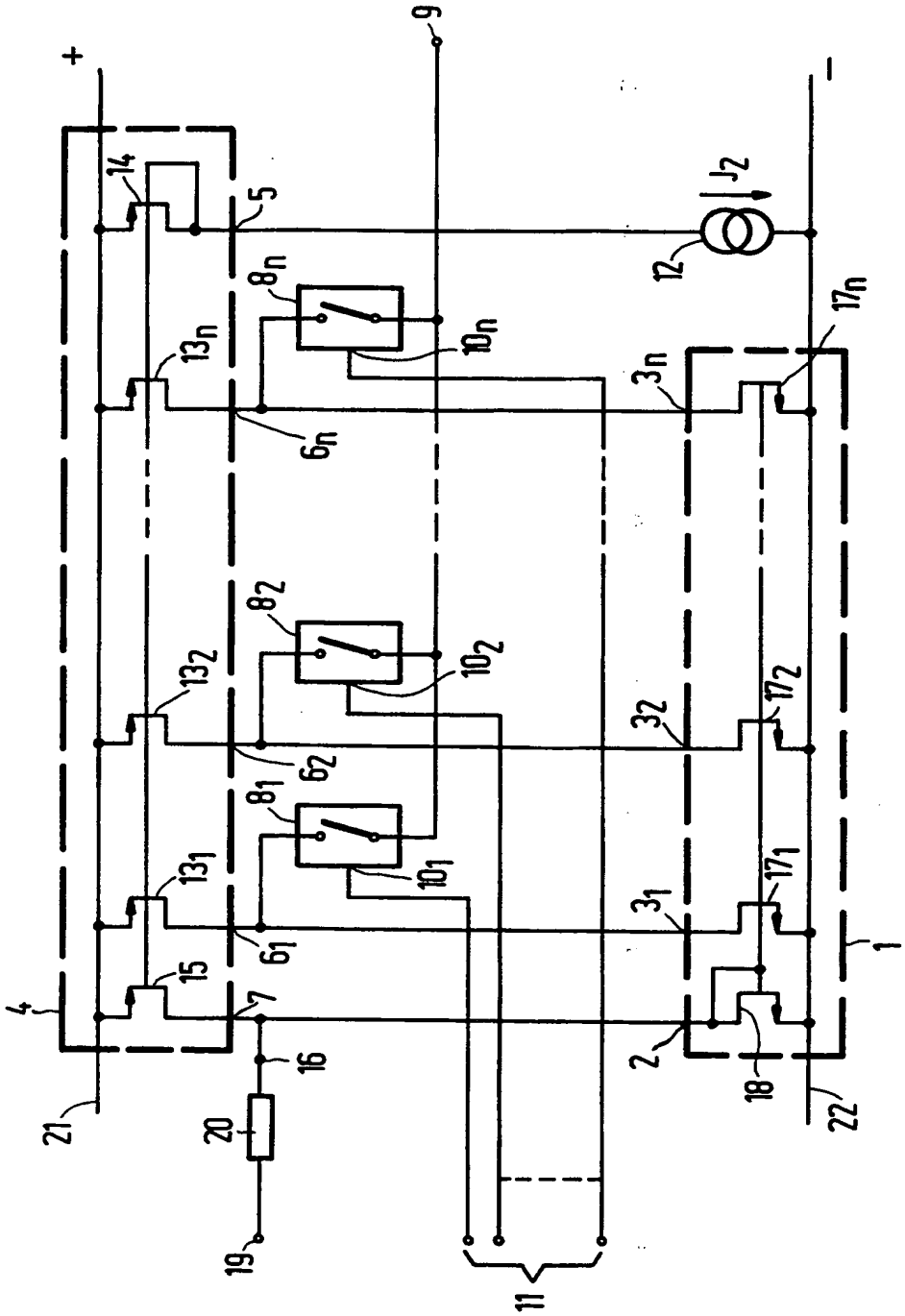

FIG.1

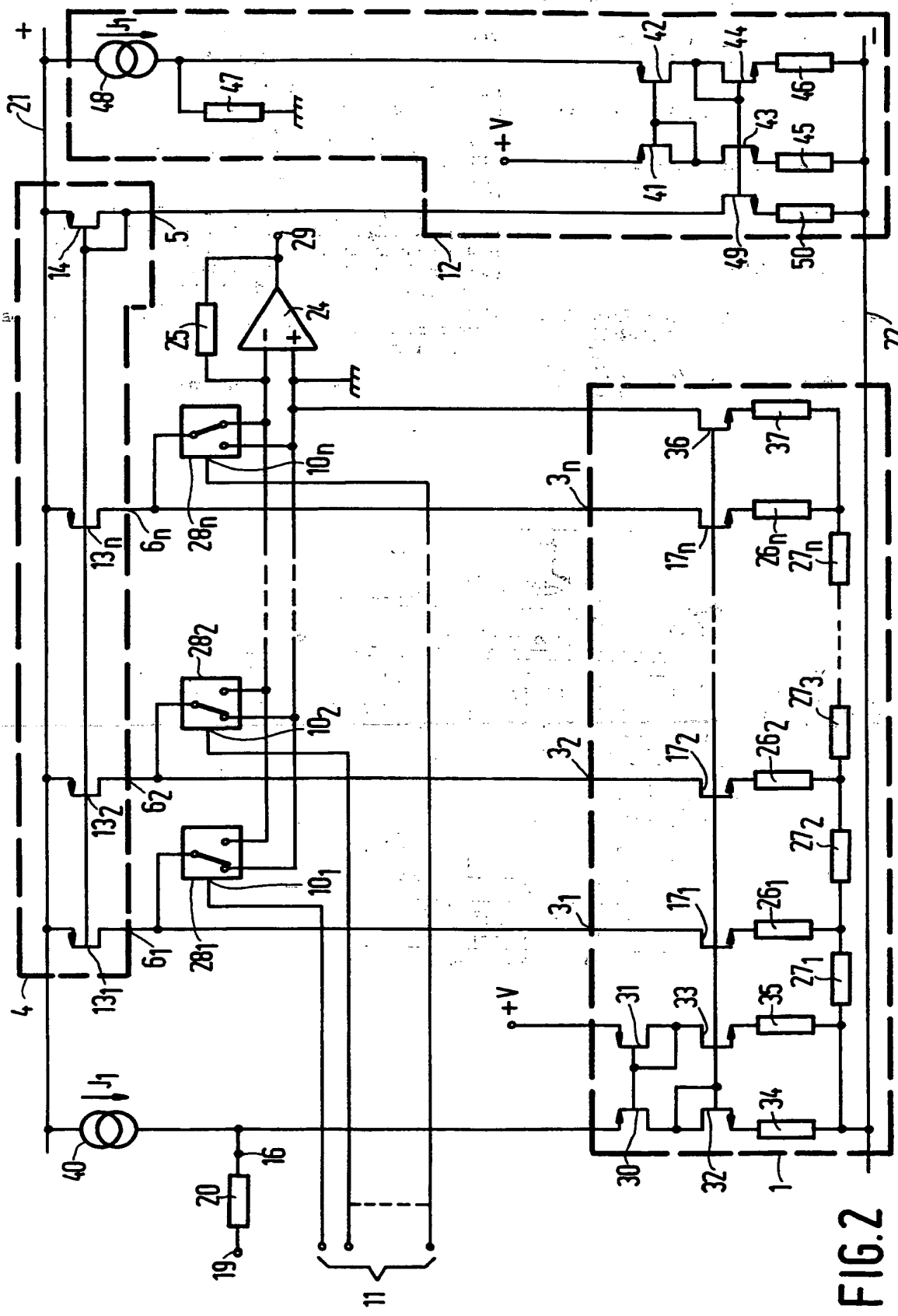

FIG.2